REMARKS

Claims 1-31 are pending in the application. Claims 1-31 are rejected.

Claims 1-11 are rejected under 35 USC 103(a) as being unpatentable over Self, US Patent No. 5,623,644 in view of Booth, US Patent No. 6,065,073.

Claims 12-31 are rejected under 35 USC 103(a) as being unpatentable over Self in view of Kelly, US Patent No. 5,379,440 and Booth.

The rejections are respectfully traversed, for the reasons cited below.

Claim 1

Independent claim 1 was rejected under 35 USC 103(a) as being unpatentable over Self in view of Booth. Applicants respectfully disagree.

Claim 1 has been amended to recite:

1. (currently amended): A computer system, comprising:

a first cluster including a first processor and a second processor of first plurality of processors and a first interconnection controller, ~~the first plurality of processors and the first interconnection controller in communication using a point-to-point architecture~~wherein the first processor is connected to the second processor through a point to point link and the first processor is connected to the first interconnection controller through a point to point link and the second processor is connected to the first interconnection controller through a point to point link;

a second cluster including a second plurality of processors and a second interconnection controller, the second plurality of processors and the second interconnection controller in communication using a point-to-point architecture, wherein disabling the second cluster comprises disabling polling for a link from the first interconnection controller to the second interconnection controller ~~can be enabled or disabled by configuring the first interconnection controller~~and flushing caches associated with the second cluster.

The combination of Self and Booth does not teach claim 1, at least because Self and Booth do not teach disabling the second cluster in the manner described in claim 1

Amended claim 1 recites "wherein disabling the second cluster comprises disabling polling for the first interconnection controller to the second interconnection controller and flushing caches associated with the second cluster."

Self and Booth do not appear to teach or suggest the disabling of clusters. Booth pertains to a "a system and method for auto-polling within a physical layer interface (PHY) to a local area network (LAN)." See Abstract of Booth. Applicants could not find a reference in Booth to a cluster or the disabling of a cluster. Self refers to micro-clusters, but appears to focus on resolving phase differences between transmitted signals. See Abstract of Self and column 1, lines 26-31. Applicants also could not find a teaching in Self of disabling a cluster. Applicants, for example, conducted a word search of Self and could not find a single instance of the terms "disable," "disconnect", "remove" or derivatives of such terms. Applicants also could not find a teaching or suggestion in either Self or Booth of the flushing of caches.

For at least the above reasons, Self and Booth do not appear to teach the claim recitation, "wherein disabling the second cluster comprises disabling polling for a link from the first interconnection controller to the second interconnection controller and flushing caches associated with the second cluster." Since the combination of Self and Booth does not appear to teach at least these features of amended claim 1, Applicants respectfully request that claim 1 be allowed.

The combination of Self and Booth does not teach claim 1, at least because Self does not teach point-to-point connections between processors

Amended claim 1 recites "wherein the first processor is connected to the second processor through a point to point link." This recitation is supported at least by Figure 2 and page 6, lines 12-14 of the present application. Page 6, lines 12-14 recite "the point-to-point communication links are configured to allow interconnections between processors 202a-202d, I/O switch 210 and interconnection controller 230." Figure 2 illustrates point to point links between processors, such as Processors 202a and 202c.

Applicants could not find a teaching or suggestion of point-to-point links between processors in Self. Page 3 of the Office Action, citing column 10, lines 35-52 and column 14, lines 1-14, asserts that Self discloses a point-to-point architecture. Column 10, lines 35-52 and column 14, lines 1-14 describe Figures 12a, 17 and 18 of Self. Figures 12a, 17 and 18 and the citations describe connections between, for example, a memory controller and processors but do not appear to teach point-to-point connections between processors. In Figure 12a, 17 and 18, processors are not drawn as having direct connections to one another.

For at least the above reasons, Self and the cited prior art do not appear to teach the claim recitation, "wherein the first processor is connected to the second processor through a point to point link." Since the combination of Self and Booth does not appear to teach at least this feature of amended claim 1, Applicants respectfully request that claim 1 be allowed.

Applicants respectfully submit that a person of ordinary skill would lack the motivation to use Booth to modify the invention of Self in the manner suggested in the Office Action

Claim 1 recites "polling for a link from the first interconnection controller to the second interconnection controller." Claim 1 was rejected under 35 USC 103 over the combination of Self and Booth. Page 3 of the Office Action states that the primary reference Self does not disclose polling from one interconnection controller to another. The Office Action suggests, however, that it would have been obvious to modify the routers/controllers of Self with the invention of Booth to implement inter-router polling. Applicants respectfully disagree, at least because Self and Booth do not appear to be combinable in the manner suggested in the Office Action.

The type of polling executed in Booth appears to be very different from the inter-router polling suggested in the Office Action. The polling of Booth is illustrated in Figure 11. Figure 11 shows an auto-polling unit 920, management interface logic 930, and a bi-directional data line (MDIO) extending from the management interface logic 930 to the auto-poll control unit 918 of auto-polling unit 920. These components are all inside network interface card (NIC) 212. Column 8, lines 32-39 describe the polling of Booth as follows:

> Generally speaking, auto-polling unit 920 monitors activity on MDIO signal 934. If no activity is detected for a predetermined number of MDC cycles, auto-polling unit 920 takes control of the management interface and queries the status register of the currently selected PHY device.

Thus, the polling in Booth appears to take place between an auto-polling unit and a management interface, both of which are contained in a single network interface card.

The routers of Self appear to have entirely different architectures. Figure 10 of Self describes such a router. Router 850, for example, comprises four pairs of point-to-point synchronous interfaces 1001-1004 operating at a 200 Mhz transmission rate, an asynchronous or synchronous interface 1005 and five identical routing blocks 1011-1015 for buffering data between each of the interface channels. See column 9, lines 51-65 of Self. Applicants respectfully submit that Figure 11 or any other part of Booth could not motivate or enable a person of ordinary skill to appropriately configure such a router for inter-router polling.

Additionally, the polling units in Booth play different roles in comparison to the routers of Self. Communications between two routers appears to entail a master-master relationship. In other words, one device in the relationship would not have unidirectional control over the other device. Booth, however, appears to teach polling between a master unit (auto-polling unit) and a slave unit (management interface). Column 8, lines 32-39, which were provided above, noted that the auto-polling unit monitors activity on a line and then "takes control of the management interface." The polling routine in master/master relationships would seem to be distinct from the polling routine for master/slave relationships. Thus, Applicants respectfully submit that a person of ordinary skill would not be motivated to use the master/slave-based polling of Booth to modify the routers of Self to conduct master/master-based polling.

For at least the above reasons, Applicants respectfully submit that a person of ordinary skill would not combine Self and Booth in the manner suggested in the Office Action. Since the rejection of claim 1 relies on the combination of Self and Booth, Applicants respectfully request that claim 1 be allowed.

Claims 12 and 23

Independent claims 12 and 23 were rejected under 35 USC 103(a) as being unpatentable over Self in view of Kelly and Booth.

Independent claim 12 is as follows:

> 12. (currently amended): A method for introducing a cluster of processors, the method comprising:
>
> configuring a first interconnection controller in a first cluster including a first plurality of processor in communication using a point-to-point architecture to poll for the presence of a second interconnection controller;
>
> asserting a reset signal on a second interconnection controller in a second cluster including a second plurality of processors in communication using a point-to-point architecture;
>
> establishing, after asserting the reset signal, a link layer protocol on a connection between the first and second interconnection controllers.

Independent claim 23, which also has been amended, is a "means for" claim including features that parallel the steps of claim 12. Thus, the arguments presented below in relation to claim 12 apply to claim 23 as well.

The cited prior art does not teach the features of claim 12, at least because Self and Kelly do not teach asserting the reset signal and establishing, after asserting reset the signal, a link layer protocol on a connection between the first and second interconnection controllers.

Claim 12 recites "asserting a reset signal on a second interconnection controller in a second cluster including a second plurality of processors in communication using a point-to-point architecture; establishing, after asserting the reset signal, a link layer protocol on a connection between the first and second interconnection controllers."

In some embodiments of the invention, the assertion of a reset signal facilitates a connection between interconnection controllers. Page 18, lines 29-32 and page 18, lines 23-28 recite:

> At 801, physical layer communications are enabled out of reset. Standard physical layer initialization sequences can be performed upon enabling the physical layer. The polling state may also be maintained... During the initialization of physical layer communications, information is exchanged between interconnection controllers. At 811, link width parameters are exchanged. At 813, link speed parameters are exchanged. At 815, optional error correction information is exchanged. At 817, the link layer is then enabled by toggling the fence bit off. With the link layer enabled, data communications can proceed.

(Emphasis added.)

To support its rejection, the Office Action argued that Self and Kelly, respectively, disclose the asserting and establishing operations of claim 12. The Office Action referred to Figure 3 of Self, which presents a block diagram of circuitry with a reset option. The Office Action also referred to column 6, lines 20-42 of Kelly, which pertains to a link protocol for communication between network elements.

Neither Self nor Kelly, however, teach or suggest a sequence of operations in which the establishing of a link layer protocol on a connection follows the asserting of a reset signal. Figure 3 of Self, for example, shows a circuit diagram with a reset option, but does not teach that such a reset option should be used before the establishing of a link layer protocol on a connection. Applicants conducted a word search of Self and could not find a single instance of the term "link layer."

Additionally, column 6, lines 20-42 of Kelly refer to a link protocol, but do not suggest associating the establishing of a link layer protocol with the asserting of a reset signal. Applicants conducted a word search of Self and could not find a single instance of the term "reset."

Thus, Applicants respectfully submit that Self, Booth and Kelly, even if combined, do not teach all the features of claim 12. In particular, Booth and Kelly do not teach or suggest following the asserting of a reset signal with the establishing of a link layer protocol on a connection. For at least these reasons, Applicants respectfully request that claim 12 be allowed.

The various dependent claims are respectfully submitted to be patentable over the art of record for at least the same reasons as set forth above with respect to their associated independent claims. Furthermore, these dependent claims recite additional features that when considered in the context of the claimed invention, further patentably distinguish the art of record.

Conclusion

Applicant's Attorney believes that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
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